AN925
Application note

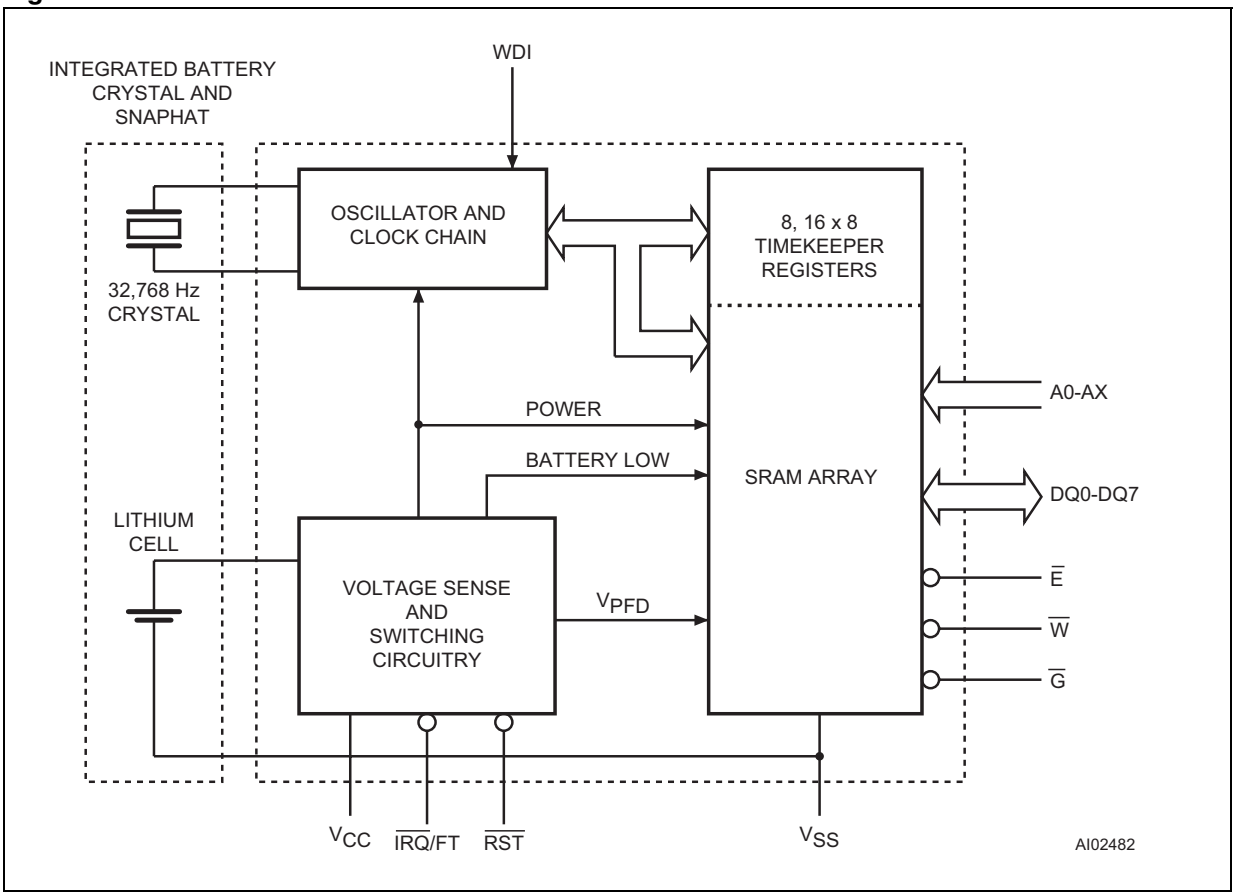
Time update in ST's TIMEKEEPER® devices

Introduction

Figure 1 shows how the non-volatile, static memory array and the quartz-controlled clock oscillator, of TIMEKEEPER® devices from STMicroelectronics, are interconnected through the clock registers. The clock registers are mapped into the memory array (please see the data sheet for the precise mapping) as 8 or 16 BYTEWIDE BIPORT memory cells. The time data in these memory cells are updated from the clock side (the system side) and are made available to the user side within the user's finest time resolution.

However, the user's finest time resolution is one second, so this leaves plenty of scope for variability (of the order of several milliseconds) between one update and the next. Since this variability might be noticeable to some applications (for example, those that poll the time registers regularly, or those that use an alarm function that is triggered once per second), this document sets out to explain the nature of the variability, to make it more predictable to the applications designer.

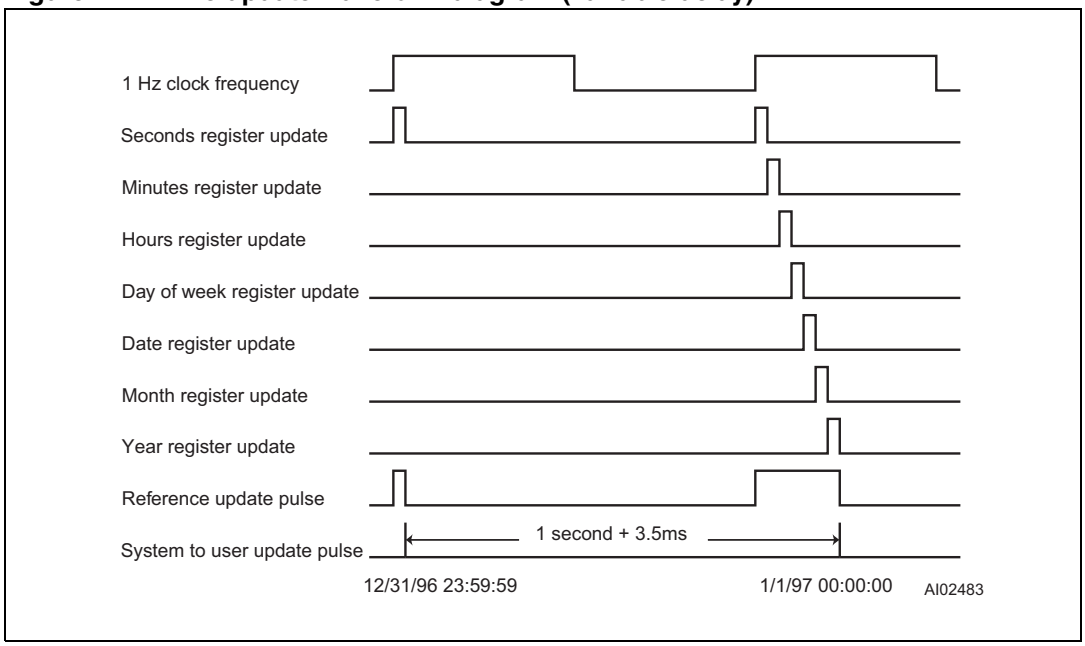
Figure 1. Internal architecture of an ST TIMEKEEPER® device



A 1 Hz clock signal, from the clock chain, is used to update the seconds register. Each rising edge of the 1 Hz clock signal increments the system side of the seconds register. Having updated the seconds register, a ripple carry to other registers might be initiated (for example, incrementing the minutes register from 00 to 01, after the seconds register has been incremented from 59 to 00). The longest possible ripple carry extends through all seven registers: seconds, minutes, hours, day of the week, date of the month, month of the year and year.

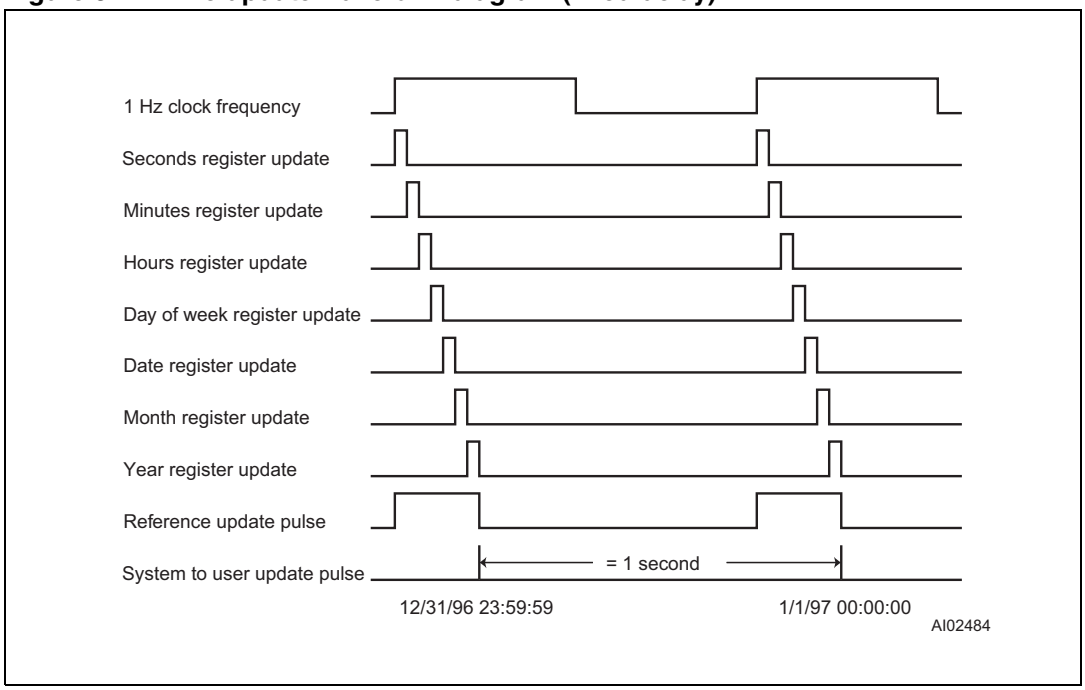
Figure 2 shows two consecutive updates of the seconds register. The first update only updates the seconds register; the second update, though, ripples through all seven clock registers. When the system-side time registers have finished being updated, they are copied across to the user-side, thereby making the updated time available to the user. Thus, the spacing between successive System-to-User-Update-Pulse is one second plus a delta delay that can vary from 0.5 ms to 3.5 ms (1x0.5 ms to 7x0.5 ms). The older M48T58 (revision B), M48T59 (revision B), and M48T559 are examples of TIMEKEEPER® devices that operate in this way.

Figure 2. Time update waveform diagram (variable delay)



An alternative approach, shown in *Figure 3*, is adopted by the newer M48T02, M48T12, M48T08/Y, M48T18, M48T58/Y (revision C), M48T35/Y, M48T35AV, M48T37Y/V and M48T201Y/V devices. The spacing between successive System-to-User-Update-Pulse is always one second. Each pulse is delayed by the same delta time, of 3.5 ms, regardless of the number of registers that need incrementing within that period.

Figure 3. Time update waveform diagram (fixed delay)



(These examples are each shown with the calibration set to zero.)

Revision history

Table 1. Document revision history

Date	Revision	Changes
Dec-1998	1	Initial release.
17-Jul-2012	2	Textual updates concerning available TIMEKEEPER® devices.

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